Nanometer Scale Electronic Device Integration Using Side-Wall Deposition and Etch-Back Technology

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Abstract

Side-wall deposition and etch-back technology is a cheap method to produce nanometer scale lines and trenches or gaps without expensive equipment like high resolution lithography or chemical-mechanical polishing. It can be used for gratings in integrated optics and in semiconductor technology for electronic device integration. This paper reflects its application for field effect transistors in bulk silicon and demonstrates its potential for nanometer scale particle transistor integration. Silicon and ZnO nanoparticle field effect transistors using different setup structures integrated by side-wall deposition and etch-back show on/off ratios of up to 4500 and mobilities up to some $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. Although the best structures apply high temperature processing, a reduced temperature process for ZnO nanoparticle transistor integration on glass and foil substrates is presented.

Keywords: nano particle transistor, deposition defined structure; nanoscale trench; ZnO.

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1 Introduction

Today the microelectronic industry needs nanometer scale geometry definition for transistor gates, contact openings and metal wiring on chips. It is performed by high resolution optical projection lithography as wafer stepper/scanner systems operating with 193 nm UV laser light illumination in combination with complex phase shifting masks, resolution enhancement structure, and immersion liquids between the projection lens and the resist surface. As demonstrated, the optical systems are capable for structure sizes of down to 22 nm [1] or even smaller. Nevertheless, the equipment and the phase shifting masks are extremely expensive. Alternatively, electron beam lithography enables direct writing of even smaller structures into thin photoresist layers [2]. Using electron beam lithography, the writing time to expose one wafer strongly depends on the focus size of the beam, which is directly correlated with the requested resolution. This leads to strongly limited wafer throughput in case of nanometer scale structure exposure. Up to now other techniques like nano-imprint lithography [3] or extreme UV lithography [4] do not fulfil the requests of low defect density or are limited by the exposure area. In 1983 Flanders [5] introduced an alternative to common lithography techniques. He used the side wall deposition and etch-back technique (SWEB) to integrate optical grids with a period of about 40 nm. In 1995 Horstmann [6] used SWEB for short channel silicon field effect transistor integration. Kallis [7] extended SWEB to local oxidation of silicon enabling MOSFET's with channel width and length below 50 nm. So far the SWEB technique was used for nanometer scale line definition down to about 15 nm, but not for openings and spaces. Carlson implemented spacings in a mask by SWEB combined with chemical mechanical polishing (CMP) [8]. As CMP is a sensitive and expensive process, it is seldom available in small companies or University research institutes. With this another way for nanometer scale trenches and openings in masks is needed. All the papers mentioned above indicate that SWEB is capable to create nanometer scale masks without complex and expensive equipment. It is a very simple approach making use of the excellent uniformity and conformity of deposition processes to define a masking layer with a structure width given by the thickness of the deposited layer. No high-resolution lithography tool is necessary, because the lithography only defines the position of the nanostructure, but not its size. This paper summarizes the current capability of the side-wall deposition and etch-back technique for microelectronic device integration on silicon and glass substrates, at reduced temperatures for devices

on foils, and extends its application range to nanometer scale space formation without CMP.

2 Processing of the Devices

2.1 Side Wall Deposition and Etch-Back

The principle of the SWEB technique is well known in microelectronic field-effect transistor integration. Here small spacers beside the transistor's gate electrode reduce the electric field in short channel field effect transistors. SWEB enables a 90 degree turn of a deposited layer structure from the lateral direction into the vertical orientation at a perpendicular step in the surface. The step can be etched directly into the substrate or into an additional sacrificial surface layer. The total process flow to create a mask by SWEB is depicted in Figure 1. Here a silicon wafer serves as the substrate, and a deposited silicon dioxide film acts as a supporting sacrificial layer to form a perpendicular step into the wafer surface. As silicon is not sensitive to high temperatures, the maximum processing temperature for SWEB is about 800°C in this case.

After cleaning of the substrate 100 nm of SiO_2 is deposited by plasma enhanced chemical vapor deposition (PECVD). Next standard optical lithography determines the position of the nanometer scale structure at the edge of

Figure 1 Side wall deposition and ... : a) deposition and b) etching of the sacrificial oxide, c) deposition of the masking layer, d) directional etch of the masking layer, e) etch of the sacrificial layer, and f) transfer of the nanostructure into the bulk material.

the developed photoresist (Figure 1a). Etching down the oxide by reactive ion etching (RIE) in CHF_3/Ar plasma gives a rectangular edge in the oxide film perpendicular to the wafer surface (Figure 1b). After resist removal conformal low pressure chemical vapor deposition (LPCVD) of silicon nitride using a $\text{SiH}_2\text{Cl}_2/\text{NH}_3$ gas mixture at 790°C follows. The uniformity of this deposition is better than $\pm 1\%$. The deposited Si_3N_4 layer thickness must be controlled carefully, because afterwards it will define the width of the mask structure (Figure 1c). The silicon nitride layer is etched back by directional etching in RIE, using CHF_3/O_2 plasma. The etching time must be chosen very carefully to remove exactly the deposited layer thickness. For safety reason an addition of 10% in time may be given (Figure 1d). With this a Si_3N_4 spacer stays back on the wafer surface, surrounding the sacrificial oxide. The width of the silicon nitride equals the deposited layer thickness because the conformity of the LPCVD process is close to one. The nanometer scale mask definition ends with a wet etching step in hydrofluoric etch solution, which removes the sacrificial silicon dioxide (Figure 1e). Due to the high selectivity of this etchant the Si_3N_4 mask is not attacked. As a result a nanometer scale Si_3N_4 mask stays back on the wafer surface. It can be transferred into the layer below by dry etching (Figure 1f). Figure 2 depicts a cross section of a crystalline silicon wafer after a deep silicon etch using SWEB for structure definition. With a Si_3N_4 mask of about 50 nm in width and 100 nm in thickness, nearly $1\text{ }\mu\text{m}$ of silicon was etched by RIE in $\text{SiCl}_4/\text{CH}_4$ plasma. Pure SiCl_4 leads to a strong directional etching profile for a depth of about 500 nm, but in larger depths an undercut of the structure occurs due to scattered ions. The addition of CH_4 leads to a passivation of the vertical side walls of the silicon structure which prevents any undercut during the etching process.

The SWEB technique can easily be transferred to generate nanometer scale lines of other materials like aluminum, tungsten, and silicon nitride or silicon oxide [9]. In case of sensitive layers the deposition temperature must be reduced by replacement of LPCVD with PECVD. In this case the limited conformity of the PECVD process requests the deposition of a thicker film as the striven mask width. The width can be calculated by the thickness of the deposited layer multiplied with the conformity factor, which is the ratio of the deposition rate at vertical surfaces to the rate at lateral surfaces.

2.2 Field Effect Transistors in Bulk Silicon

For field effect MOS transistor's gate definition the SWEB technique is used on top of the polycrystalline silicon film, which is deposited for the transistor

Figure 2 (a): crystalline silicon nanostructure fabricated by a deposition defined mask using the side wall deposition and etch-back technique and reactive ion etching of silicon in $\text{SiCl}_4/\text{CH}_4$ plasma, and (b): 60 nm polycrystalline silicon gate structures with a Si_3N_4 mask on top on 4.5 nm gate oxide for field effect transistor integration.

gate electrode formation. As thermal stability and etchant selectivity are nearly the same for polycrystalline silicon and bulk silicon, the process as described above is transferable without any changes to the top of the polycrystalline silicon. Figure 2 at the (b) shows an example of 60 nm wide polycrystalline silicon gate electrodes on 4.5 nm gate oxide, used for NMOS transistor integration. Although the line width is very uniform on the whole 4" wafer, the structure itself is a little bit wavy. This is caused by the surface roughness of the polycrystalline silicon film in combination with the limited perfection of the resist mask on top of the sacrificial oxide. It results in small lateral fluctuations in the position of the nanometer scale lines. The imperfectness of the resist structure comprises in an edge angle of a little bit less than 90° after development and hard bake. The wavy form can be avoided by improving either the surface roughness of the polycrystalline silicon film or by optimization of the resist mask angle, e.g. by reducing the post exposure bake temperature. For NMOS transistor integration, after polysilicon gate etching, a lightly doped

drain profile was created by antimony (Sb) ion implantation with 15 keV at a dose of $3 \cdot 10^{12} \text{ cm}^{-2}$. Side wall spacers were created by depositing 110 nm of SiO_2 and subsequent directional dry etch back of the layer. Drain/source implantation uses arsenic (As) with 60 keV and a dose of $5 \cdot 10^{15} \text{ cm}^{-2}$.

Figure 3 at the (a) depicts the output characteristics of an NMOS transistor ($W/L = 300 \text{ } \mu\text{m}/70 \text{ nm}$, $t_{\text{ox}} = 4.5 \text{ nm}$) in bulk silicon, integrated using SWEB technique and doping profiles as described above. The device enables a stable operation range up to a drain-source voltage of 3 V. The characterization of the MOSFETs on wafer level (100 mm diameter) indicate a high yield in operating devices with well-defined and extremely uniform transistor's channel length, which allows to analyze statistical parameter fluctuations

Figure 3 (a): output characteristics of a NMOS transistor ($W/L = 300 \text{ } \mu\text{m}/0.07 \text{ } \mu\text{m}$, $t_{\text{ox}} = 4.5 \text{ nm}$) integrated by SWEB, and (b): Standard deviation of the threshold voltage and the transconductance in neighboring identical transistors in dependence on the active channel area (data include characterization of more than 4.000 transistors).

[10, 11]. For example, in Figure 3 (b) the standard deviation of the threshold voltage and of the maximum conductivity of neighboring identical transistors are depicted in dependence on the total active channel area. Both parameters are linear in dependence on $1/(W \cdot L)^{0.5}$.

2.3 Single Nanoscale Particle FET Devices

For a long time the SWEB technique was not capable to generate a mask layer for nanometer scale gaps or trenches without CMP. To compensate this disadvantage additional processing steps were introduced to transform small lines into small spacings. One way to do this is the application of the evaporation technique at high vacuum condition. During evaporation the vaporized material moves on a straight line from the source to the substrate without any interaction with atoms of the residual atmosphere. If a substrate is oriented perpendicular to the direction of the source, the particle beam will condensate on planes with a component in source direction only and not on planes perpendicular to the wafer surface. According to this, the sidewalls of the nanometer scale line in Figure 4a will not be covered with the evaporated material. If the nanometer scale structure formed according Figure 1 is higher than the evaporated layer, a part of the line will rise out of the deposited film (Figure 4b). Applying a selective isotropic etchant, it is possible to remove the material of the line out of the film, which results in a nanometer scale trench (Figure 4c). Those trenches in metal layers can be used for field effect transistors made of silicon or zinc oxide nanoparticles. These transistors use SCHOTTKY contacts formed by aluminum to semiconductor transitions from drain and source metal contact to the semiconducting nanoparticles.

The typical setup of such a nanometer scale particle transistor device is an inverted coplanar structure as depicted in Figure 5a. It consists of a glass or foil substrate with an evaporated gate metal like titanium, titanium nitride or aluminum. The gate metal is insulated by plasma-deposited CVD or by

Figure 4 Additional process steps for the transformation of the nanoscale line into a nanogap.

Figure 5 (a) Inverted coplanar setup of the nanoparticle transistor using SCHOTTKY contacts for drain and source, (b) Nanometer scale trench in an aluminum film of 100 nm in thickness, integrated by SWEB.

spin-coating of a special insulating resin. On top of the dielectric layer the side wall deposition and etch-back process starts to integrate a nanometer scale line of SiO_2 above the center of the gate electrode. Because of the restricted temperature stability of the substrate, photoresist must be used as the sacrificial layer, and low temperature PECVD SiO_2 serves as the mask material [12]. As the conformity of the PECVD deposition is limited at about 100°C , the layer thickness must be about twice of the nanometer scale line width. Etch-back of the mask forming layer happens by RIE, the removal of the sacrificial layer occurs in a solvent like acetone.

The nanometer scale line is transformed into a trench next. This is done by e-beam evaporation of about 40 nm aluminum at high vacuum conditions. After selective removal of the PECVD oxide line the deposited aluminum can serve as source and drain electrodes of the field effect transistor. Figure 5(b) depicts a nanometer scale trench integrated in an evaporated aluminum film, measured by atomic force microscopy. To complete the transistor device the

space in the metal film must be filled with semiconducting particles matching the trench width. This can be done by spin-coating of a dispersion containing nanoparticles of ZnO or Si as the last process step. Some of the particles penetrate into the trench and form the active semiconducting material of the field effect transistor. Figure 6(a) shows the output characteristics of a ZnO transistor formed by spin-coating of a water based ZnO dispersion (mean particle size: 100 nm). The output characteristic depicts an n-type field effect transistor with a threshold voltage of about -0.5 V and an on/off-ratio of about 4500. The calculated charge carrier mobility on the base of the metal gap width of 100 nm results in a low mobility of about $0.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Although the output characteristic confirms transistor behavior, only a few of the metal templates really form transistor devices. The nanometer scale particles prefer to form a bridge on the top of the metal gap and do not tend to penetrate into the trench. According to this preference, one can assume that operating devices consist of only one or two particles acting as a transistor. With this assumption the mobility of the charge carriers in the ZnO particles would be in the range of 10 to $20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. At the highest gate voltage it is conspicuous to see some strong fluctuations in the drain current. According to vidor [13] there exist a large number of traps at the interface semiconductor to the gate dielectric layer, which can be charged and discharged in a time scale of around 0.5–3 s. These traps are responsible for a hysteresis in the transfer characteristics of the devices, causing a threshold voltage shift of some volts depending on the history of the gate voltage.

As silicon is the most common material for FET devices, the dispersion of ZnO is replaced by an ethanol based dispersion with silicon nanoparticles (mean particle size: 60 nm). In this case the trench width, formed by SWEB, is chosen to be 60 nm, the transistor width is 800 μm . The ethanol solvent vaporizes very fast causing a strong particle agglomeration on top of the trenches, which reduces the yield in operating devices even more than in case of ZnO particles. The few operating transistor devices show p-type characteristics with low drain currents, and the calculated charge carrier mobility is $0.015 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. One reason may be the natural oxide shell surrounding the silicon nanoparticles, which result in potential barriers in the metal contact areas. This is supported by the weak growth of the drain current in case of low drain voltages. On the other hand, as only very few devices are operating, one can assume again, that only one particle in the trench is active. At a channel length of 60 nm the active transistor width can be estimated to be 60 nm, too, although the metal trench width is 800 μm . With this, the mobility increases by a factor of more than 10^4 to about $200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$; this is

Figure 6 (a) Output characteristic of a ZnO nanometer scale particle transistor consisting of a 100 nm wide gap partly filled with ZnO particles between source and drain, and (b) Output characteristic of a Si nano particle field effect transistor with a distance of 60 nm between drain and source metal.

an acceptable value for p-type silicon transistors. To increase the number of operating devices the inverted staggered setup according to Figure 7(a) was analyzed. In this case the SWEB technique must be applied on top of the nanoparticle film; this is critical due to the limited adhesion of the particles in case of low temperature processing. Nevertheless, after sintering at 150°C the particle film is capable to withstand the needed process steps including optical lithography.

Figure 7(b) depicts the output characteristics of the corresponding nanoparticle transistor. The number of operating devices has strongly increased, and the transistors seem to use the total width of the contact metals. This results in a drain current in the μA range, although the charge carrier mobility is in the range of $10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ only. The low mobility may result from the natural oxide shells surrounding the silicon particles. Due to the oxide the current is limited by potential barriers between the particles. Nevertheless, this will reduce the current by one or two orders of magnitude, but not down to the measured value. Another effect is the effective insulator thickness. As the coated particle film is about some micron in thickness, only the top particles lead to the current flow. This effect strongly increases the

Figure 7 (a) Inverted staggered setup of the single nanoparticle field effect transistor and (b) Output characteristics of this FET with $W/L = 800 \mu\text{m}/0.07 \mu\text{m}$, $t_{\text{ox}} = 30 \text{ nm}$, using undoped Si nanoparticles.

dielectric layer thickness, which limits the transistor current again by about two orders of magnitude.

2.4 Nanoparticle Based TFT Transistors

Using a noninverted staggered setup for the nanometer scale particle transistors the yield in operating devices is much higher. Here the ZnO nanoparticle film is coated onto the substrate directly after the formation of the source and drain contacts with nanometer scale gap.

After a thermal treatment at about 150°C, on top of the nanoparticle film the gate dielectric layer is deposited by spin coating, and the gate metal is evaporated. The setup is depicted in Figure 8(a). In this case the channel length,

Figure 8 (a) Noninverted staggered field effect transistor structure for nanoparticle transistors on insulating substrates, and (b) Output characteristics of a ZnO FET with $W/L = 20 \mu\text{m}/0.3 \mu\text{m}$, $t_{\text{ox}} = 120 \text{ nm}$, in noninverted staggered setup.

Figure 9 ZnO transistors with aluminum electrodes on a glass wafer.

integrated by SWEB technique, was 300 nm. As the mean ZnO particle cross section is 100–120 nm, the charge carrier transport between drain and source includes multiple particles. Figure 8(b) depicts the output characteristics of a FET device with $W/L = 20\text{ }\mu\text{m}/0.3\text{ }\mu\text{m}$ on glass substrate using the noninverted staggered setup. Due to the potential barriers at the inter particle transitions the drain current is in the nA range only. Nevertheless, nearly all devices are operating, and the calculated mobility for electrons is about $2 \cdot 10^{-4}\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$. Figure 9 shows a photo of the glass wafer with ZnO nanoparticle transistors integrated by SWEB using the non-inverted staggered device setup. The only non-transparent areas consist of the aluminum metallization level. Replacing the aluminum by transparent conductive oxides like indium-tin-oxide or fluorinated tin oxide, completely transparent microelectronic circuits can be integrated.

3 Conclusion

Up to now SWEB is used in research groups as a cheap and simple method to replace common high resolution lithography techniques. With this, field effect transistors are integrated in bulk silicon with very uniform channel length, which allows the determination of statistical effects on transistor parameters. The SWEB technique basically enables the formation of nanometer scale lines, but additional steps transform these lines into metal gap

structures for electronic device integration on different kind of substrates. New application areas for these uniform gaps are nanometer scale particle transistors integrated on oxidized silicon, glass or foil substrates. Here first operating devices on the base of silicon and ZnO nanoparticles are demonstrated using different setups for the transistor devices. In inverted coplanar technique the total yield in operating devices is low at moment. To increase the yield the filling of the trenches must be improved in further research work. Inverted and noninverted staggered devices show high yields. Problems arise from interparticle transitions, which form potential barriers for the charge carriers. In conclusion SWEB enables the formation of high resolution nanometer scale line and space masks with high reproducibility at very low cost.

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Biographies

U. Hilleringmann studied physics from 1978 to 1984 at University of Dortmund, Germany. From 1984 to 1985 he was with the Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany. Afterwards Hilleringmann changed to the Department of Electrical Engineering at University of Dortmund, where he wrote a thesis about “Laser Recrystallization of Silicon” in 1988. In 1994 he received the “*venia legendi*” at the same department with the corresponding thesis “Integrated Optics

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Gilson I. Wirth received the B.S.E.E and M.Sc. degrees from the Universidade Federal do Rio Grande do Sul, Brazil, in 1990 and 1994, respectively. In 1999 he received the Dr.-Ing. degree in Electrical Engineering from the University of Dortmund, Dortmund, Germany. Since January 2007 he has been professor at the Electrical Engineering Department at the Universidade Federal do Rio Grande do Sul - UFRGS. From 2000 to 2002 he worked as lecturer and researcher in the field of microelectronics at the Informatics Institute, Universidade Federal do Rio Grande do Sul (UFRGS). From July 2002 to December 2006 he was professor and head of the Computer Engineering Department, Universidade Estadual do Rio Grande do Sul (UERGS). He founded the research group in micro- and nano- electronics at UERGS. In July, August and December 2001 he was at Motorola, Austin, Texas, leading the team working in CMOS process technology transfer to CEITEC, Porto Alegre, Brazil. The technology transfer was funded by FAPERGS under grant number 01/1093.3 (first phase of technology transfer) and 01/1628.9 (second phase of technology transfer). In February and March 2002 he was at the Corporate Research Department of Infineon Technologies, Munich, Germany, working as guest researcher on low-frequency noise in deep submicron MOS devices. His research work is focused on reliability and yield of MOS devices and circuits, including low-frequency noise, bias temperature instability (BTI), radiation effects, and design techniques to improve yield and reliability.