Hardware Implementation of Three Phase Five-level Inverter with Reduced Number of Switches for PV Based Supply

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Abstract

This paper proposes a three phase five-level inverter which uses a single DC (PV) source, unlike a conventional cascaded H-bridge (CHB) which requires multiple DC (PV) sources, and also a novel Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) for reduced voltage Total Harmonic Distortion (THD) compared to a conventional SHE-PWM. The proposed inverter uses reduced number of switches when compared to conventional inverter. The proposed three phase inverter is simulated in MATLAB with both conventional and new SHE-PWM techniques. The simulated waveforms of the line, phase voltages and load current are studied in detail. A comparison of THD values is for both conventional and proposed SHE-PWM is presented. This is followed by the hardware implementation of the proposed inverter with the new SHE-PWM, and the results for line, phase voltages and the load currents are again reviewed. The hardware results are found to match the simulation results. The results confirm that the proposed SHE-PWM has the ability to deliver a reduced THD when compared to a conventional SHE-PWM.

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Keywords: Five-level inverter, Single DC source, Conventional Selective Harmonic Elimination, New Selective Harmonic Elimination, Total Harmonic Distortion, Photo-Voltaic (PV).

1 Introduction

Multilevel inverters (MLIs) can deliver high voltage with low total harmonic distortion at reduced switching frequency, using low voltage switching devices. Therefore, MLIs have found widespread acceptance in medium and high voltage applications like solar and wind power applications [3, 4, 18–22]. The desired power rating can be achieved without increasing the individual device rating by just increasing or decreasing the number of levels. The more the number of levels, the lower the harmonic content of the output voltage [1, 2]. A m-level inverter produces a phase voltage of m-levels and a line voltage of (2m-1) levels hence; multilevel inverters have the advantage of having less distortion of line voltage.

The common topologies of MLI are Diode Clamped/Neutral Point Clamped (NPC) multilevel inverter, Flying Capacitor (FLC) multilevel inverter and Cascaded H-Bridge (CHB) multilevel inverter. Of these three categories, the CHB inverter is the simplest to design, as they do not require clamping diodes and capacitors. The inverter consists of $\frac{(m-1)}{2}$ isolated DC sources and 2(m-1) IGBT/diode pairs for an m-level inverter. High voltage is achieved by cascading multiple single-phase inverter modules [5]. It offers better flexibility, robustness and is easier to control. The only drawback of the CHB inverter is its requirement of a separate DC source for each H-bridge leading to increased cost [6–8] and it requires 2(m-1) number of switches for m-level. Cascaded inverters with a single DC in which, the circuit uses only one DC source irrespective of number of levels are discussed by the authors in [23] and [24], but the number switches used remain the same as the conventional cascaded inverter. A MLI with a single DC source is proposed with one DC source, but for other stages, capacitors are used which increases the components [25]. Two H-Bridges are connected in series with the second one fed from a capacitor acting as a DC sources instead of DC supply [26]. The paper also proposes a new topology of inverter with single DC source and reduced number of switches and a novel SHE-PWM to achieve a lower THD value.

Section 2 of this paper discusses the proposed five-level CHB inverter with a single DC source. The new SHE-PWM is described in Section 3, simulation and experimental results are dealt in Section 4 and the conclusions is presented in Section 5.

2 Proposed Five-level CHB Inverter with Single DC Source

The paper proposes a new inverter topology which removes the necessity of separate DC sources. The inverter uses only one DC source irrespective of number of levels and number of phases. It uses $\frac{(m-1)}{2}$ number of transformers for an m-level inverter. The single phase circuit of the proposed five-level CHB inverter with a single DC source is shown in Figure 1.

This inverter uses only (m-1) switches to implement the m-level inverter and a single DC source. It uses 2 three winding transformers, with two primary windings and one secondary winding. The DC source is connected to the primary side of the transformer through the switches. The secondary windings and the load are connected in series. The switching states to get the five levels of output voltages are given in Table 1.

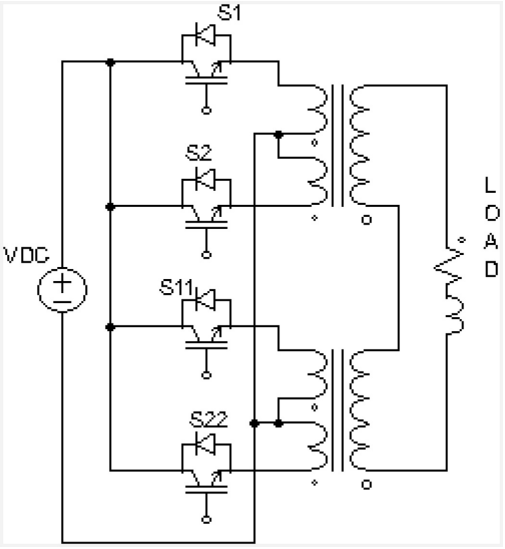

Figure 1 Single phase five-level inverter with single DC input.

Table 1 Switching states of proposed inverter

Output Voltage/Switches	S_1	S_2	S_{11}	S_{22}
$+V_{DC}$	ON	OFF	OFF	OFF
$+2V_{DC}$	ON	OFF	ON	OFF
0	OFF	OFF	OFF	OFF
$-V_{DC}$	OFF	ON	OFF	OFF
$-2V_{DC}$	OFF	ON	OFF	ON

The various modes of operation are discussed below.

- Mode 1 (S_1-ON): In mode 1 S_1 is ON, the source current follows the 1st primary winding of the first transformer and the direction of the load current is illustrated in Figure 2. The output voltage is positive and is equal to V_{DC} since the turns ratio is one.
- Mode 2 (S_1, S_{11}-ON): In this mode, both S_1 and S_{11} are ON, the source current flows through the 1st primary windings of both the transformers and the load current is also shown in Figure 3. The output voltage is positive and is equal to 2 V_{DC}.
- Mode 3 (S_2-ON): In mode 3 S_2 is ON, the source current flows through the 2nd primary winding of the first transformer and the direction of the load current is illustrated in Figure 4. The output voltage is negative and is equal to $-V_{DC}$.
- Mode 4 (S_2, S_{22}-ON): In this mode, both S_2 and S_{22} are ON, the source current flows through the 2nd primary windings of both the transformers and the load current is shown in Figure 5. The output voltage is negative and is equal to $-2V_{DC}$.

The three phase topology of proposed inverter as shown in Figure 6 requires 3(m-1) numbers of switches while the conventional inverter requires 6(m-1) numbers of switches. Again, the proposed topology uses a single DC source

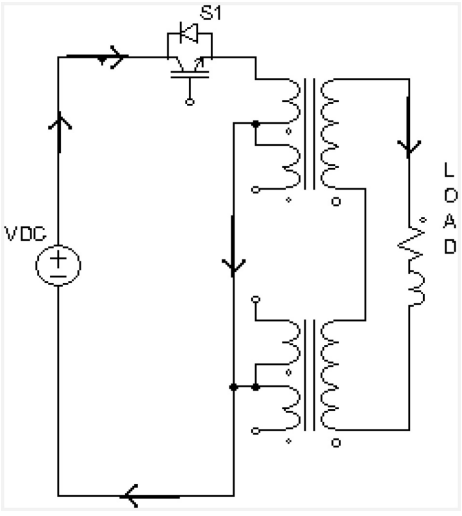

Figure 2 Mode 1.

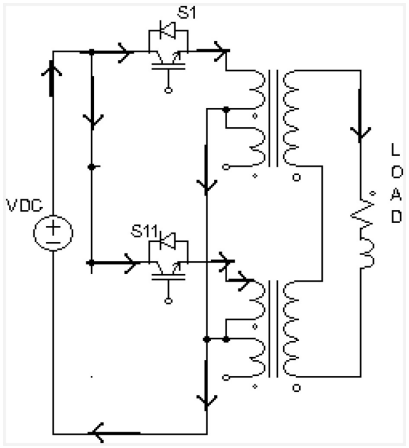

Figure 3 Mode 2.

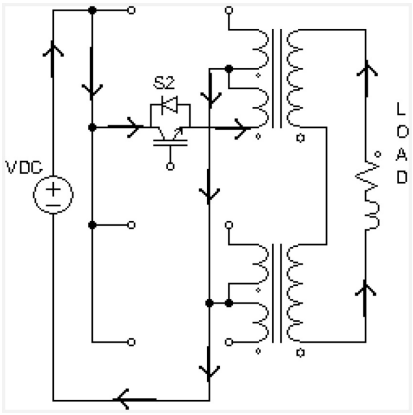

Figure 4 Mode 3.

irrespective of number of levels, whereas the conventional three phase inverter requires $3\frac{(m-1)}{2}$ number of DC sources.

3 New SHE-PWM

Among the PWM techniques, the multicarrier PWM technique is the most popular. But this technique utilizes a high frequency carrier signal thus increasing switching losses. Hence, ideally a PWM technique at the fundamental

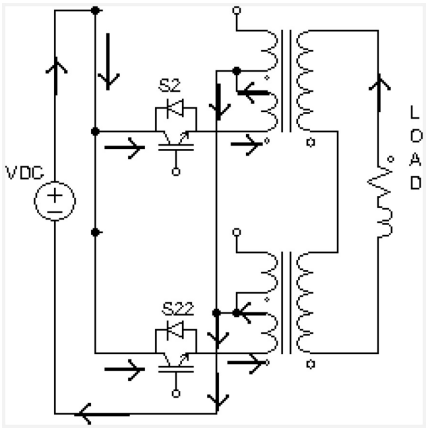

Figure 5 Mode 4.

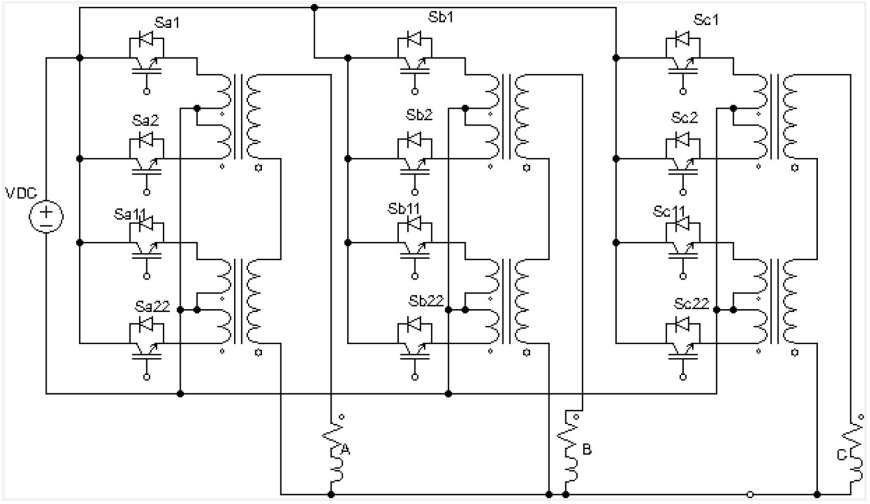

Figure 6 Three phase five-level inverter with single DC.

frequency is desired. Selective harmonic elimination at fundamental frequency is found to be the best suited PWM technique. This technique has the ability to generate the desired fundamental value by eliminating dominant lower order harmonics [9–11]. It can also determine switching angles by solving a set of non-linear transcendental equations [12–17]. Two transcendental equations are solved to compute two switching angles for a five-level inverter.

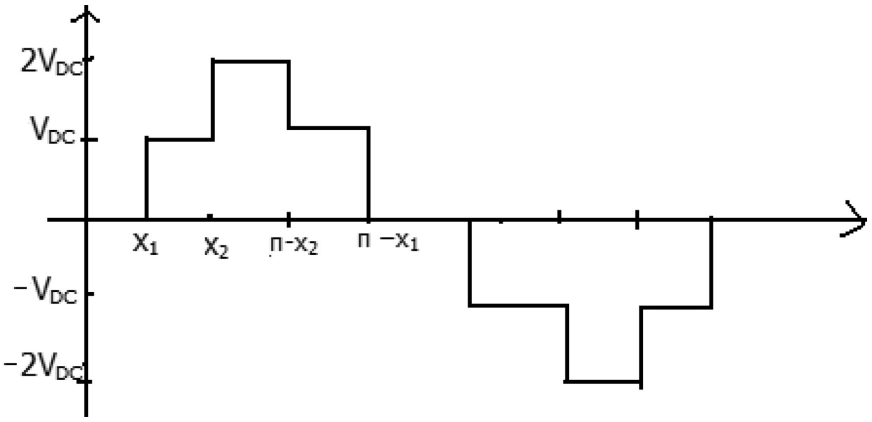

Figure 7 Five-level inverter output voltage Vs switching angles.

The Newton-Raphson method, known for its fast iterations, is chosen to solve the two equations using initial approximate values.

Figure 7 illustrates the output voltage waveform of the five-level inverter for a full-cycle. This staircase waveform can be expressed using Fourier series as given by Equation (1).

$$v_a(\omega t) = \sum_{n=1,3,5\ldots}^{\infty} \frac{4V_{DC}}{n\pi} \left(\cos\ n\theta_1 + \cos n\theta_2\right) \sin(n\omega t) \tag{1}$$

Where θ_1 and θ_2 represent the switching angles, and $0 < \theta_1 < \theta_2 < \pi/2$. From (1) the fundamental voltage can be expressed as:

$$V_1 = \frac{4V_{DC}}{\pi}(\cos\theta_1 + \cos\theta_2) \tag{2}$$

The maximum value of the fundamental voltage obtainable is, $V_{m1} = \frac{4sV_{DC}}{\pi}$, where $s = \frac{(m-1)}{2}$ for a m-level inverter. In order to eliminate the desired harmonic, for example the third harmonic, $n = 3$ is substituted and is equated to zero as in Equation (4). The switching angles for the conventional SHE-PWM (C-SHE-PWM) for a five-level inverter are calculated using the fundamental and the third harmonic Equations (3–4).

$$\cos(\theta_1) + \cos(\theta_2) = \frac{\pi V_1}{4V_{DC}} \tag{3}$$

$$\cos(3\theta_1) + \cos(3\theta_2) = 0 \tag{4}$$

Solving the equations using the Newton-Raphson method, the switching angles are at $\Theta_1 = 0.1306$ radians and $\Theta_2 = 0.9166$ radians. Hence, the third harmonic is eliminated while the higher order harmonics are retained. Minimization of fifth order harmonic and elimination of third harmonics is done by considering fifth harmonic equation along with the third harmonic equation and ignoring the fundamental one. The fifth harmonic equation equated to a minimum value is given by (5).

$$\cos(5\theta_1) + \cos(5\theta_2) = 0.0001 \tag{5}$$

Solving Equations (4) and (5), the switching angles for the new SHE-PWM are found to be $\Theta_1 = 0.2094$ radians and $\Theta_2 = 0.8378$ radians. When the switches are triggered with these angle values, the voltage THD is found to be lower than that produced with a C-SHE-PWM.

4 Simulation and Experimental Results

The proposed topology of the single phase five-level inverter is simulated for both C-SHE-PWM and the new SHE-PWM techniques with RL load of 750 Ω, 240 mH. The generated waveforms for output voltage, output current and the FFT analysis are obtained for both. Figure 8 shows the output voltage and output current of the inverter, and Figure 9 shows the THD of the output voltage and current for the C-SHE-PWM. Figure 10(a) show the output voltage and output current of the proposed five-level inverter for the new SHE-PWM with RL load of 750 Ω, 240 mH. The phase angle between voltage and current for the same is theoretically calculated to be 0.3189 msec as illustrated in Figure 10(b). Figure 11 shows the THD of the output voltage and current for the new-SHE-PWM.

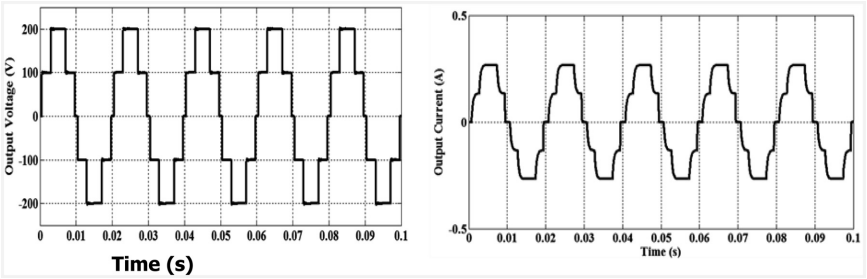

Figure 8 Output voltage and Output current for C-SHE-PWM.

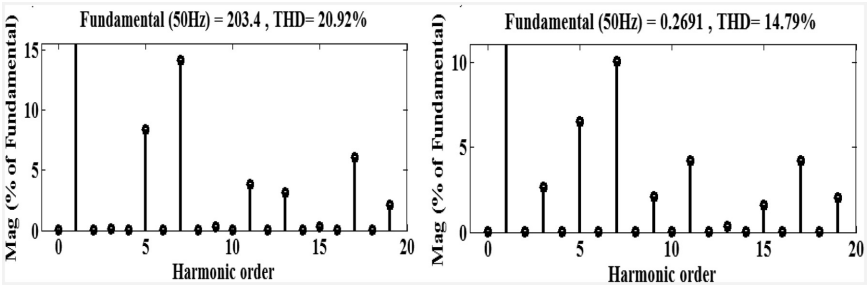

Figure 9 THD of the output voltage and current for C-SHE-PWM.

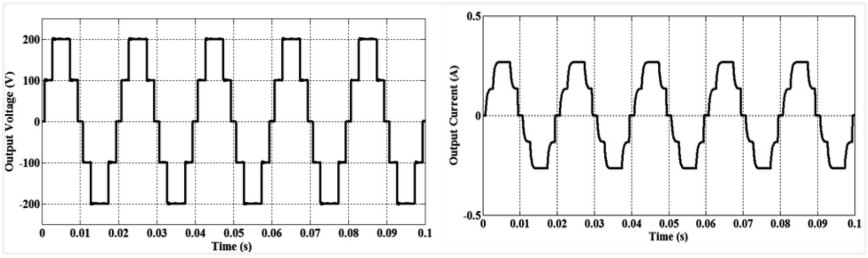

Figure 10(a) Output voltage and current for the new SHE-PWM for RL load.

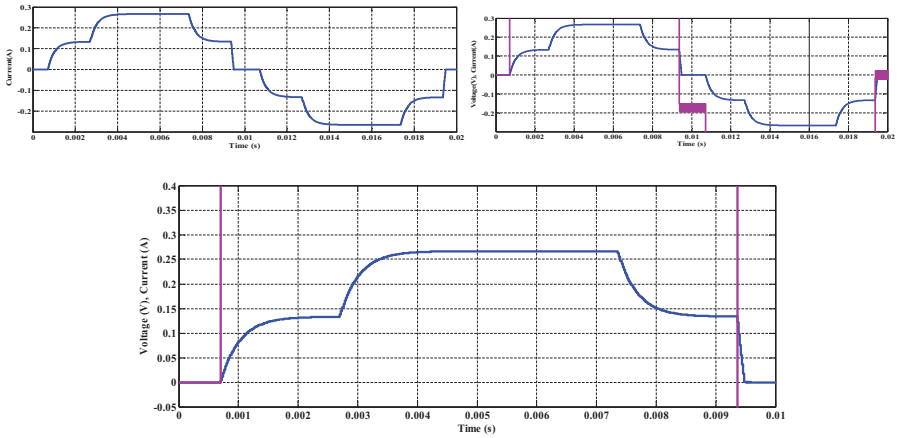

Figure 10(b) Output current for the new SHE-PWM for RL load.

From Figure 9 it is observed that fundamental voltage and current are of magnitude 203.4 and 0.2691 respectively, furthermore the 2^{nd}, 3^{rd}, 4^{th} order harmonic in voltage is zero while in current it is 0, 2.5 and 0 respectively

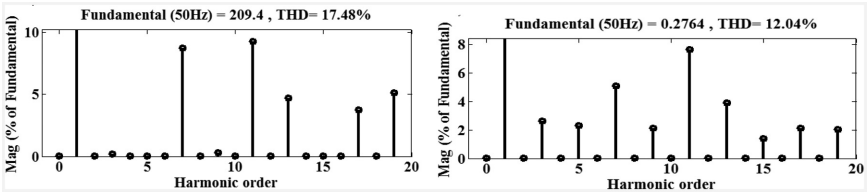

Figure 11(a) Output phase voltage and current THD for the new SHE-PWM.

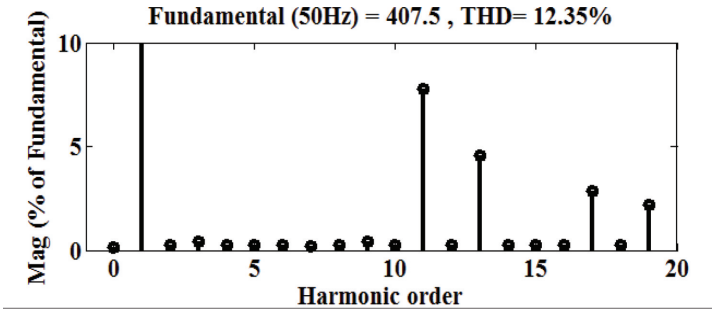

Figure 11(b) Output line voltage THD for the new SHE-PWM.

for SHE-PWM. The 5^{th} order harmonic of voltage and current is 8 and 7 in magnitude. The illustration in Figure 11(a) depicts that the THD of the new SHE-PWM in 2^{nd}, 3^{rd}, 4^{th}, 5^{th} and 6^{th} order harmonic for voltage is zero, while for current the values are 0, 2.5, 0, 2 and 0 respectively. This clearly proves that 5^{th} voltage order is mitigated in the new SHE, while it is of 8 magnitude in C-SHE-PWM. Similarly in current harmonic it is reduced from a magnitude of 7 to 2.5.

Figures 8 and 11, depicting the simulated waveforms of the phase voltage THDs, it can be deduced that the C-SHE-PWM produced a voltage THD of 20.92% whereas the proposed new SHE-PWM resulted in a phase voltage THD of 17.48% and the line voltage THD is 12.35% (Figure 11(b)). This proves that with the new SHE-PWM, the THD value is lesser when compared to the conventional one.

The three phase circuit of the proposed five-level inverter is also simulated in MATLAB/Simulink with star connected RL load of 750 Ω, 240 mH/phase. The waveforms of the output voltages and currents are shown for the new SHE-PWM.

Figure 12 shows the line and phase voltage waveform of the three phase five-level inverter for the new SHE-PWM. Figure 13 shows the load current

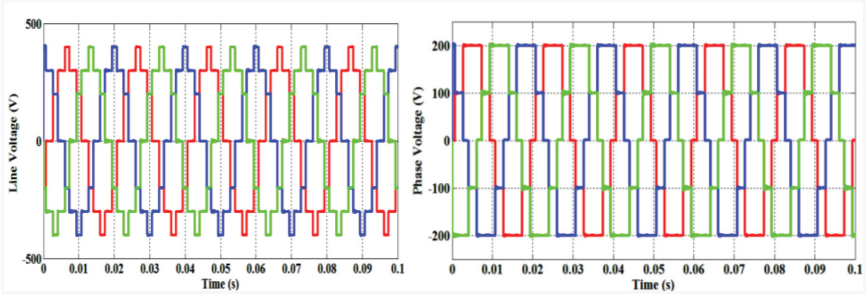

Figure 12 Three Phase line and phase voltage for the new SHE-PWM.

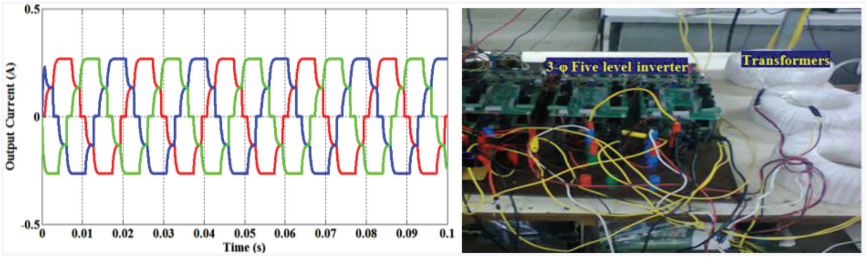

Figure 13 Three phase Load current for the new SHE-PWM for RL load and Experimental set-up.

of the three phase five-level inverter with new SHE-PWM for the RL-load and its experimental set-up.

The proposed five-level inverter is implemented in hardware with IGBT/Diode pairs. The inverter is switched with the switching angles generated with the new SHE-PWM. The switching patterns are generated in the field programmable gated array (FPGA) board. The FPGA is used to generate 12 PWM signals with 4 PWM signals for each phase. The inverter is experimentally verified with 3-φ RL-load. Figure 14 shows the experimental single phase output voltage and current waveforms for a RL load of 750 Ω, 240 mH/phase. Toroidal transformers with ferrite core are used and hence losses are kept to minimum. Though the size increases, the number of switches used and hence the associated losses are decreased.

Figure 15 shows the experimental waveforms of voltage and current THDs of the proposed MLI for the new SHE-PWM. From the Figures 11(a) and 15 it is realized that the voltage THD of the MLI is 17.48% for simulated output voltage and 17.471% for the experimental output voltage, and hence the

new SHE-PWM is found to be satisfactory. From Figures 11(a) and 15, it is also found that the current THD for the RL load obtained in simulation is 12.04%, while the experimental value is 12.116%, which is almost close to the simulated value. Table 2 shows the comparison of voltage THDs for simulated results and experimental results of the proposed inverter.

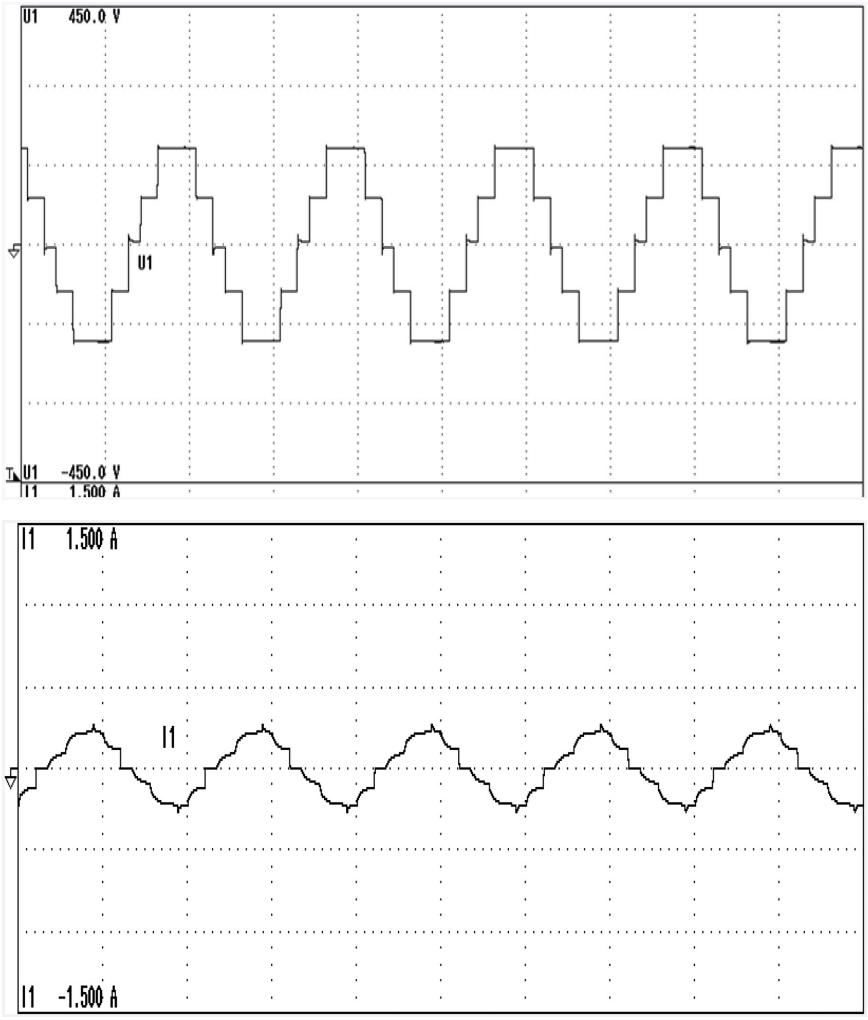

Figure 14 Experimental output voltage and current with new SHE-PWM.

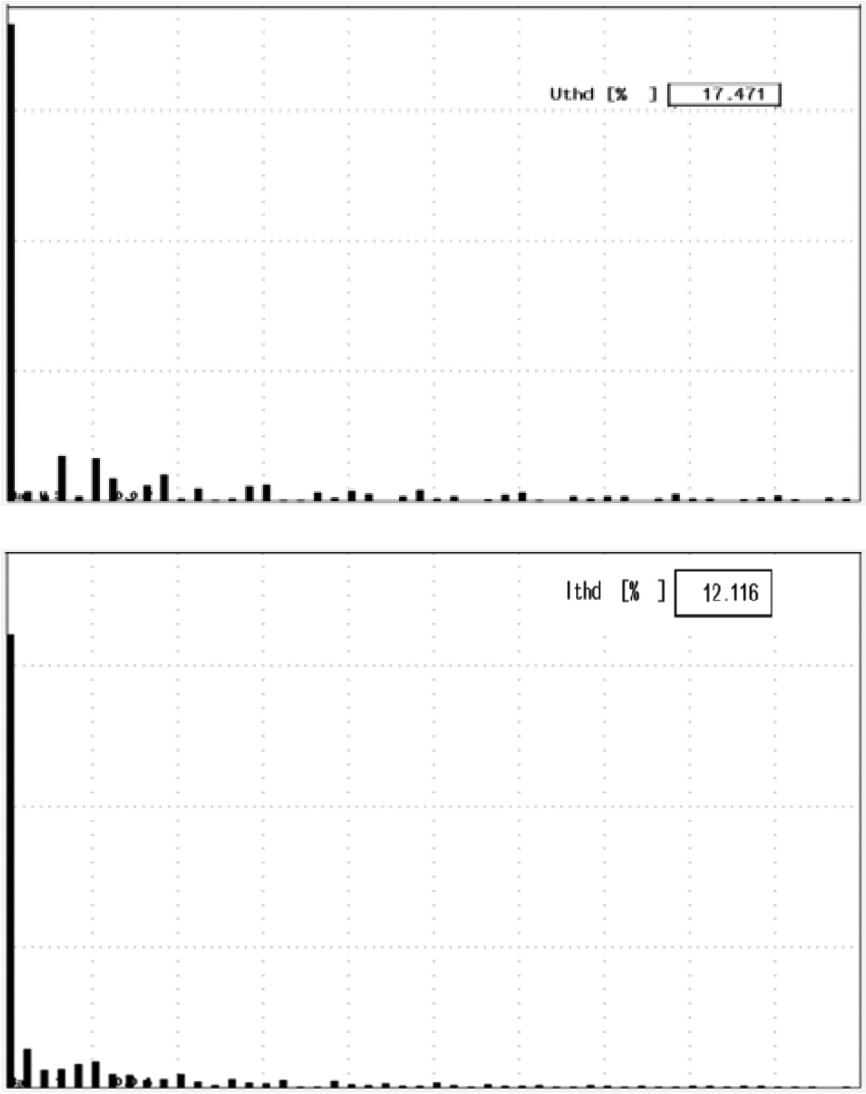

Figure 15 Voltage and current THD of MLI for with new SHE-PWM.

Figure 16 show the phase and line voltage waveforms for the three-phase five-level inverter for the new SHE-PWM. Figure 17 shows the load current of the three-phase five-level inverter with the new SHE-PWM with RL-load.

Table 2 Comparison of voltage THDs

Type	Value (%)
Simulated value of voltage THD with C-SHE-PWM	20.92
Simulated value of voltage THD with new SHE-PWM	17.48
Experimental value of voltage THD with new SHE-PWM	17.471

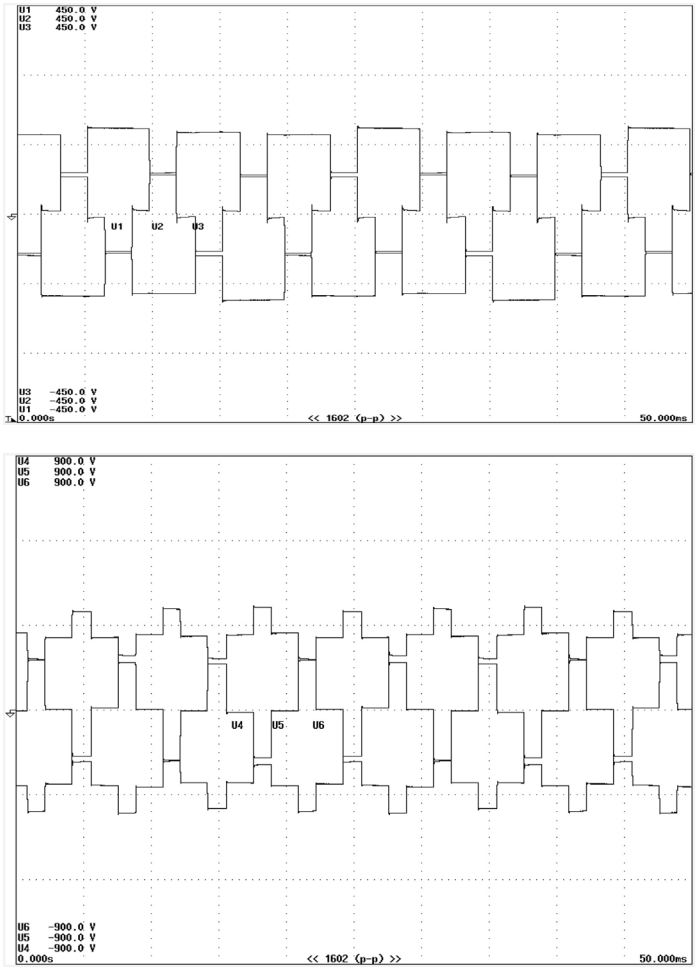

Figure 16 Three Phase and line voltage with the new SHE-PWM.

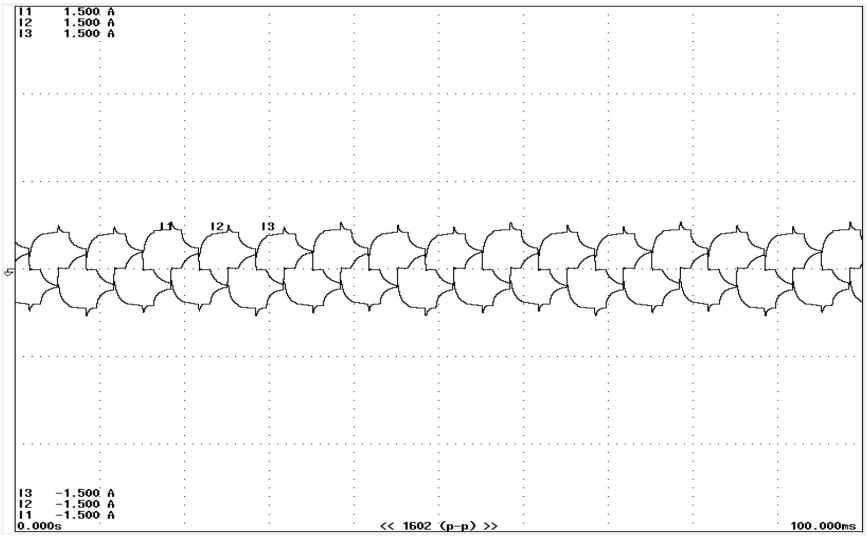

Figure 17 Output/load current of the three-phase five-level inverter with the new SHE-PWM for the RL load.

5 Conclusion

A new topology of CHB MLI with a single DC and reduced number of switches is proposed to overcome the disadvantage of the conventional CHB inverter. The proposed topology employs a single DC source, irrespective of number of levels and phases. A new SHE-PWM is also proposed which eliminates one more harmonic component, i.e., for a five-level inverter, the C-SHE-PWM eliminates only the 3^{rd} harmonic, but the proposed SHE-PWM eliminates the 5^{th} harmonic also in addition to 3^{rd} harmonic. The simulation is carried out for a single phase inverter with RL-load for both the SHE-PWMs. The voltage, current, voltage THD and current THD are obtained for both the SHE-PWMs. The proposed three phase five-level inverter is also simulated with the new SHE-PWM and the simulated waveforms of phase voltage, line voltage and the line currents are obtained for RL-load. From the waveforms obtained, we can arrive at the conclusion that the new SHE-PWM produces lower THD when compared to that with the C-SHE-PWM. The proposed three phase MLI is also implemented in hardware and verified experimentally with RL-load using the new SHE-PWM. The experimental waveforms of the voltage, current and the THDs are obtained and analyzed. Using the results generated from the proposed CHB inverter with single DC source, we can conclude that using the new SHE-PWM design results in reduced voltage THD.

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