

## **PART II**

### **Development of Multi-Sensor Data Acquisition System**

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## Outline of System

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### 3.1 High Level Input Specification

A high level draft technical specification was provided by Turbomeca as the basis for the design of the high temperature electronics platform. The design concept was to take the output from several on-engine sensors (temperature probe, thermocouple, strain gauges, frequency), carry out the signal conditioning on the sensor signals, multiplexing, analogue to digital conversion and transmission of the data through a serial data bus. The DC power supply for the unit is provided by the FADEC. The unit has to meet the environmental requirements of DO-160 for a helicopter engine, with the specific need to operate at 200°C, with short term operation at temperatures up to 250°C. The system service lifetime target is 50,000 engine flight hours.

### 3.2 Technology Assessment and Selection

A review of the options for the high temperature electronics to be considered for the HIGHTECS module was carried out. This review included the availability of devices and components, the status of high temperature electronics packaging technology, an assessment of the technology maturity, potential failure modes and a review of accelerated life tests to predict service life.

For the electronic devices and components, an ASIC based on a Silicon-on-Insulator (SOI) semiconductor manufactured using the X-FAB 1 μm SOI foundry in Germany was selected to perform the analogue signal conditioning, multiplexing, ADC (Analogue to Digital Conversion), logic control and serial data transmission. The circuit also required additional high temperature voltage regulators, a clock oscillator, capacitors, precision resistors and lightning protection devices, all of which should be capable of meeting the high temperature operating conditions. The review highlighted the limitations of ceramic based capacitors and Si based lightning protection

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devices. High temperature silicon capacitors produced by Ipdia – France became available during the course of the project and development SiC transient voltage suppressors, which have potential for operation above 150°C were evaluated.

The status of high temperature electronics packaging for the HIGHECS module was also reviewed, covering materials and processes for die attach and wire bonding, attachment of passive devices and packaged components to ceramic substrates and connections for external inputs/outputs to/from the HIGHECS module. An assessment of potential failure modes relating to the packaging technology options was undertaken, which highlighted areas to focus on within the testing programme.

The review covered the use of accelerated reliability tests to predict service life. In conclusion, the following tests were defined to address the concerns for the reliability of the electronics components and packaging technology operating at high temperature:

- Long term temperature storage at +250°C to assess the long term degradation at temperature
- Rapid thermal cycling from -40°C to +225°C to represent the stresses endured during the typical flight profile
- Vibration at room temperature and at 200°C to investigate whether the combined effect of vibration and temperature accelerates any failure mechanism

Tests have been carried out to investigate these factors on a SOI test chip.

### **3.3 Definition of Prototype System**

The design principle of the HIGHECS module was based on a custom silicon on insulator (SOI) ASIC being used for the majority of the signal processing and conditioning from the range of sensors (i.e. temperature probe, strain gauges, thermocouple, frequency), multiplexing, analogue to digital conversion and transmission of data through an ARINC 429 databus. The ASIC was then integrated with a high temperature external clock and packaged onto a ceramic hybrid circuit. This hybrid circuit was assembled in a Kovar package together with development high temperature SiC based transient voltage suppressors, which was hermetically sealed in an inert gas atmosphere. The Kovar package was then mounted into a stainless steel enclosure containing high temperature connectors and EMI shielding.

### 3.3.1 HIGHTECS SOI ASIC

The ASIC block diagram for the HIGHTECS module is presented in Figure 3.1. From the analogue sensor outputs (temperature probe, strain gauges, thermocouple), the signals pass through buffers/low pass filters for conditioning and then into a 10:1 analogue multiplexer. The output from the analogue multiplexer is fed to an analogue to digital converter which outputs to the ARINC 429 bus.

From the frequency outputs (Nfreq and Qfreq), the signals are processed using comparators/counters, synchronised with an external clock and sent to a 16b digital multiplexer. The DIN input is also sent to the digital multiplexer. The digital multiplexer outputs to dual ARINC 429 buses. The ARINC 429 bus is the selected serial output from the HIGHTECS module.

The functional blocks for the HIGHTECS ASIC are presented in Table 3.1.

A picture of the 1<sup>st</sup> version of the HIGHTECS ASIC is presented in Figure 3.2. The ASIC contains all the sensor conditioning circuits, ADC,

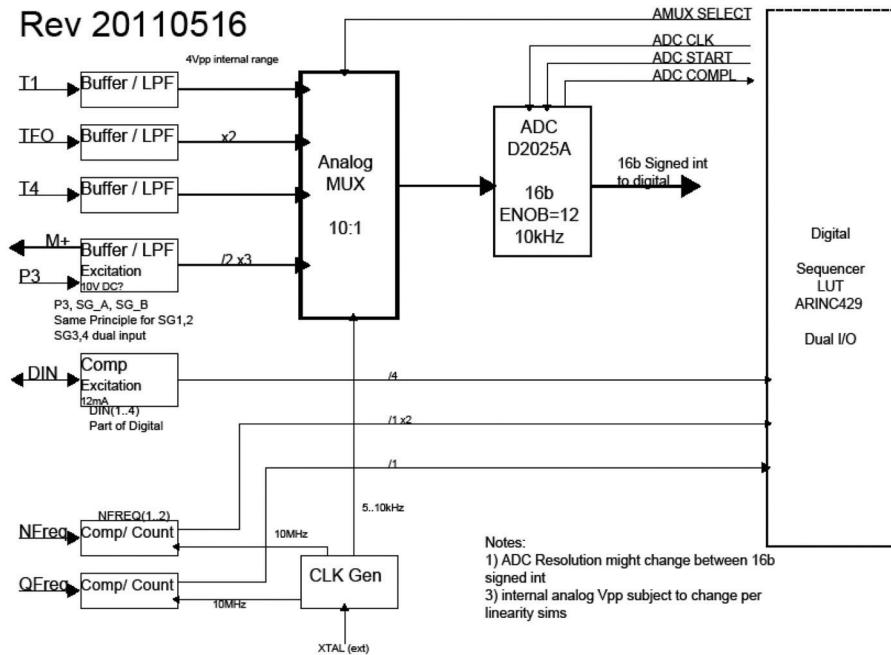
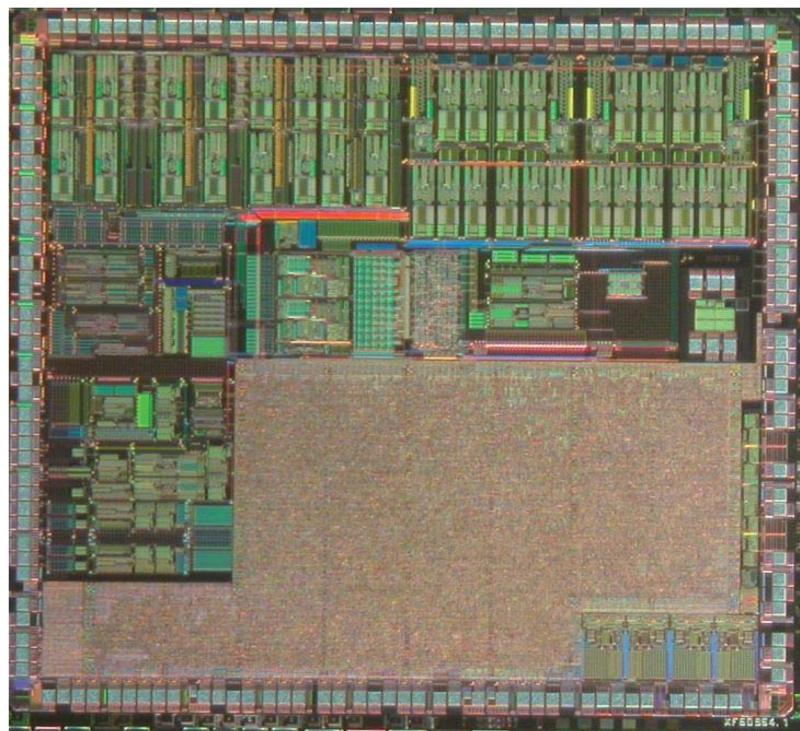


Figure 3.1 Block diagram for SOI ASIC in HIGHTECS module.

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**Table 3.1** Functional blocks for HIGTECS ASIC

| Block Name | Block Name                  |
|------------|-----------------------------|
| SG1        | Bandgap                     |
| SG2        | Global current mirrors      |
| P3         | Voltage generator           |
| T4         | Reference current generator |
| T1         | ARINC Driver (x2)           |
| TFo        | DIN (4i/ps)                 |
| NFreq      | ARINC Control sequencer     |
| QFreq      | Nfreq & Qfreq logic         |
| ADC        |                             |



**Figure 3.2** 1<sup>st</sup> Version of HIGTECS ASIC – device size 7.48 mm × 5.95 mm.

Multiplexer, Qfreq and Nfreq measurement and dual ARINC 429 outputs.  
The die size is 7.48 mm × 5.95 mm.

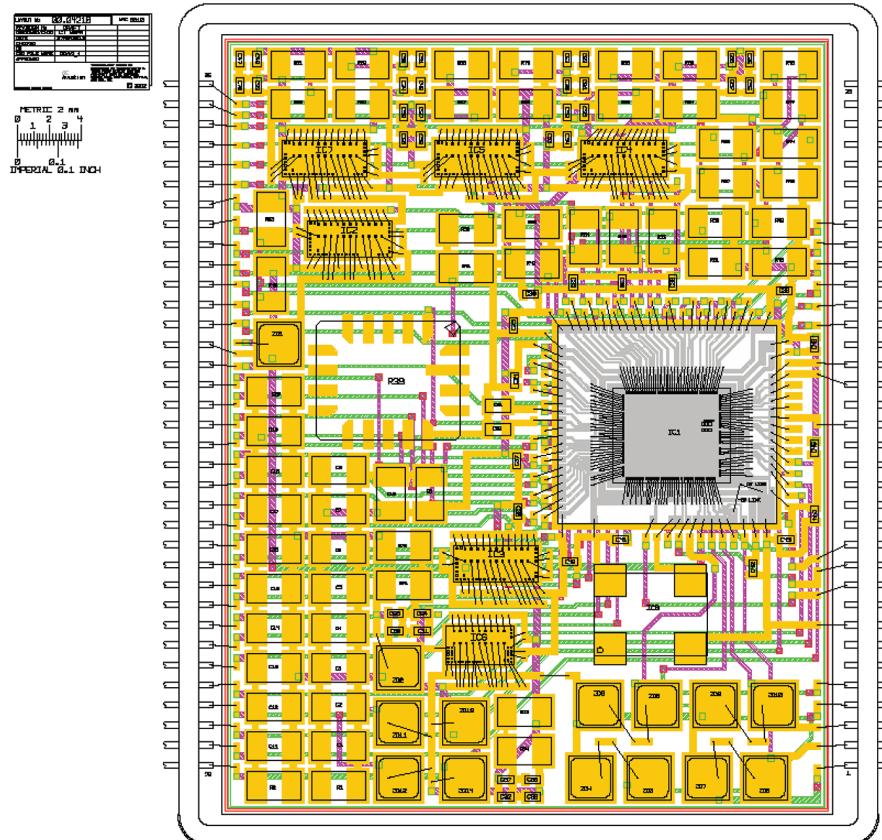
The 2<sup>nd</sup> version of the HIGTECS ASIC was re-laid out and manufactured at Xfab, a die picture is shown in Figure 3.2. Modifications were made to the layout of the connections to the ADC including bringing

out of voltage references, and changes to the VHDL code for Tfo2 and Nfreq.

### 3.3.2 HIGHECS Hybrid Circuit

The HIGHECS hybrid circuit layout is presented in Figure 3.3. The hybrid circuit contains the following components in addition to the HIGHECS SOI ASIC:

- Voltage Regulators
- External Clock Generator/Crystal Oscillator
- Prototype SiC Transient Voltage Suppressors
- Resistors
- Capacitors



**Figure 3.3** Layout of HIGHECS hybrid circuit.

In addition to the hybrid circuit a high temperature printed circuit board containing resistors required for the frequency sensors was designed and manufactured. This board was also mounted in the HIGHECS module.

### **3.3.3 HIGHECS Module**

A drawing of the HIGHECS module assembly is presented in Figure 3.4.

The hybrid circuit (containing the ASIC) sealed in a hermetic Kovar package and the high temperature printed circuit board (containing resistors) is mounted into the stainless steel enclosure. A clamping plate is used to fix the Kovar package in place.

The stainless steel enclosure is completed by mechanical fixing of a lid with an EMI shielding gasket to the stainless steel base. Future versions may be welded, but, at this stage, a removable lid is preferred.

Two connectors are used; one for the sensor input signals and power supply, the other for the ARINC 429 serial databus outputs and connections. For the high temperature application, stainless steel based connectors are commercially available with an upper temperature limit of 260°C.

Filtering on the connector for improved EMC and lightning protection is not proposed at this stage for the HIGHECS module. Based on the signal voltages and frequencies, additional filters may be required for future versions of the HIGHECS module, which will be inserted between the connector pins and the leads on the Kovar package.

## **3.4 Manufacture of Prototypes**

### **3.4.1 HIGHECS ASIC in PGA Package**

A picture of a Si wafer containing the HIGHECS ASIC is presented in Figure 3.5. After initial probing, the wafer containing HIGHECS ASIC was sawn into individual die and assembled into a 181 I/O High Temperature Co-Fired Ceramic (HTCC) Pin Grid Array (PGA) package using die attach, aluminium wire bonding and Au-Sn solder lid sealing in an inert atmosphere, see Figure 3.6. The devices have been used for functional, characterisation and environmental testing.

#### **3.4.1.1 HIGHECS hybrid circuit**

The prototype hybrid circuit design was laid out for manufacture on a 96% alumina substrate. The circuit was built up using Au thick film and dielectric layers and the resultant substrate is shown in Figure 3.7.

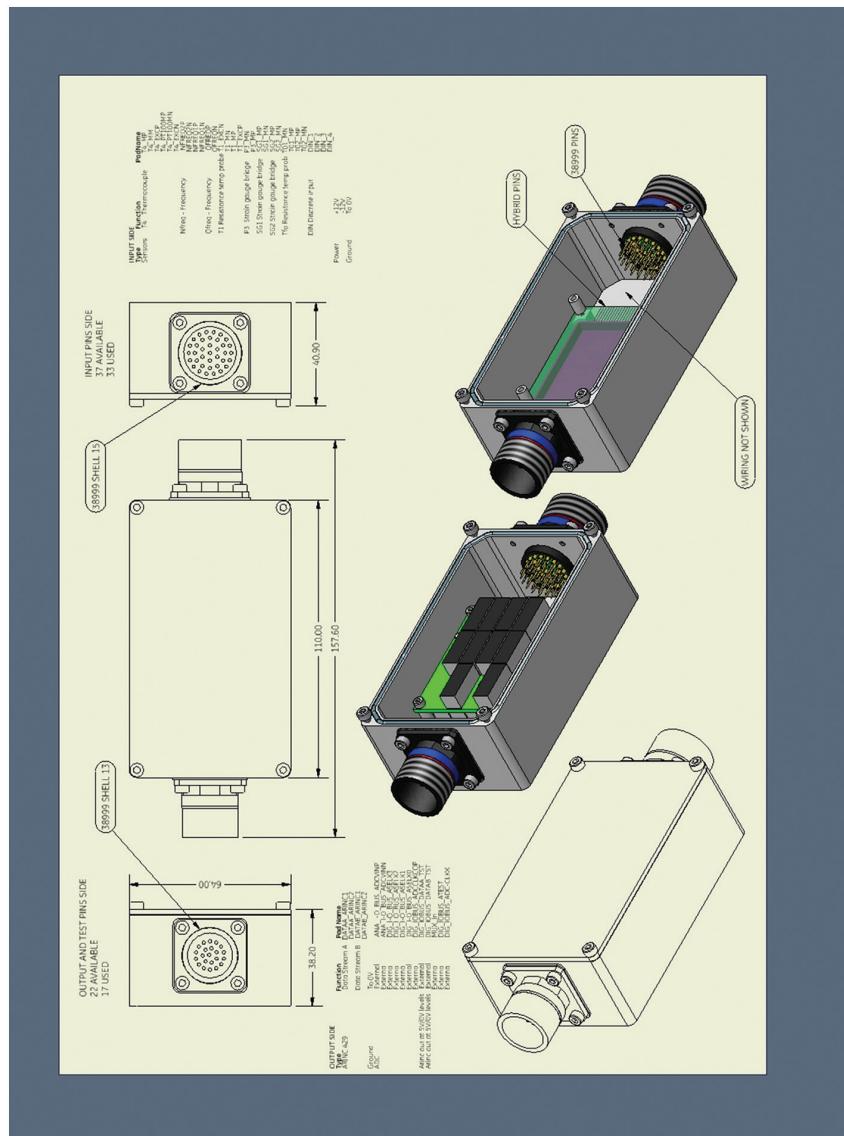
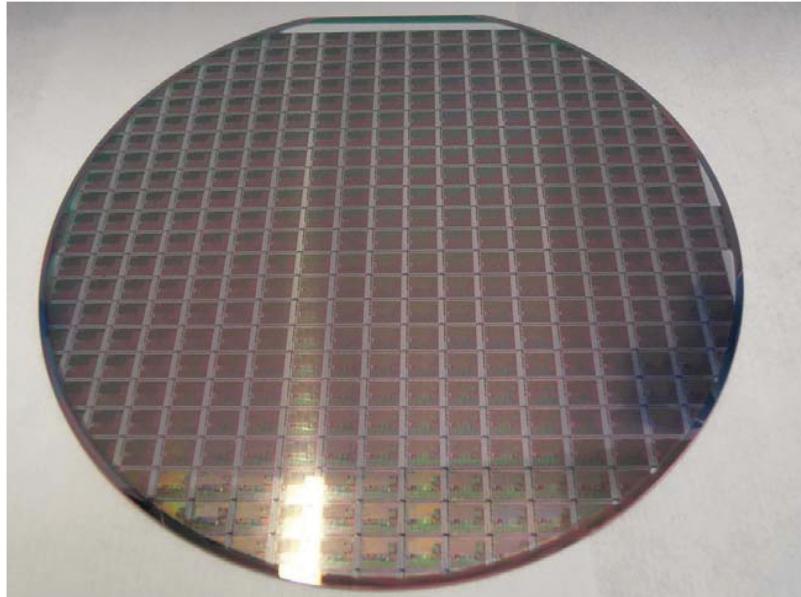
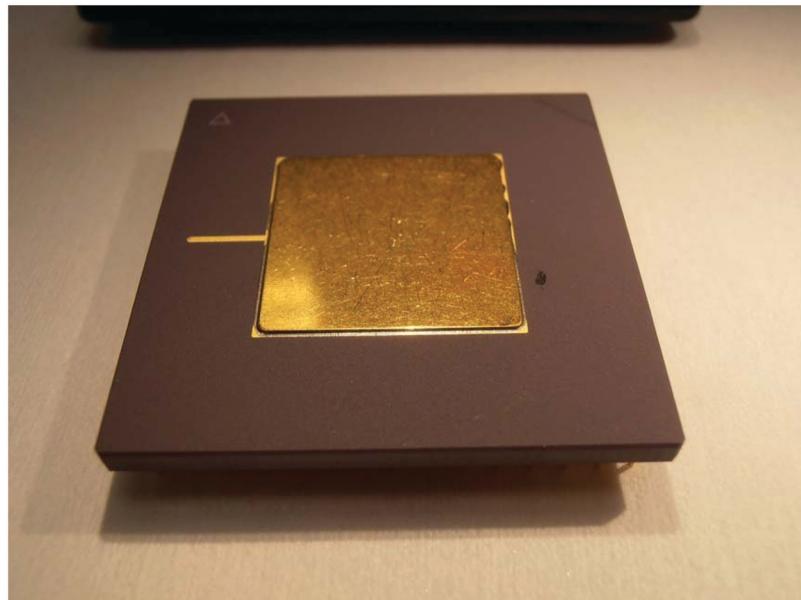


Figure 3.4 Mechanical assembly drawing for HIGHTECS module.

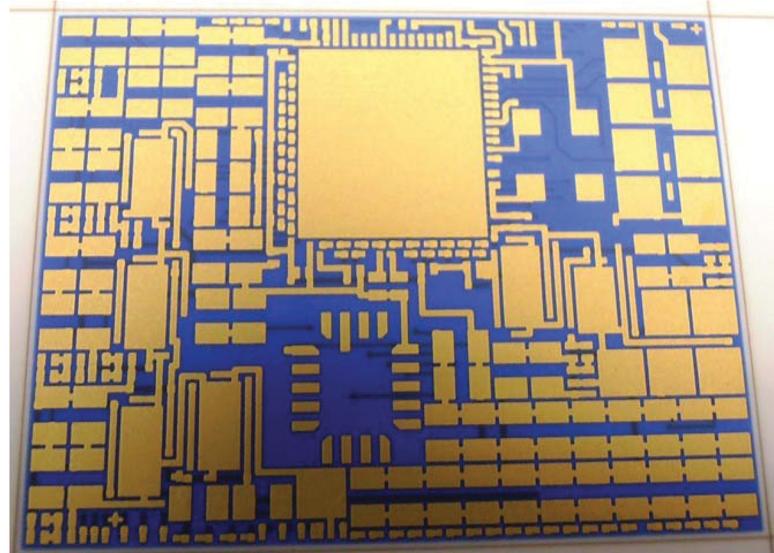
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**Figure 3.5** Silicon wafer containing HIGHECS ASICs.



**Figure 3.6** HIGHECS ASIC assembled in HTCC PGA package.



**Figure 3.7** HIGHECS hybrid circuit substrate.

The following components were assembled onto the substrate and the populated substrate is shown in Figure 3.8.

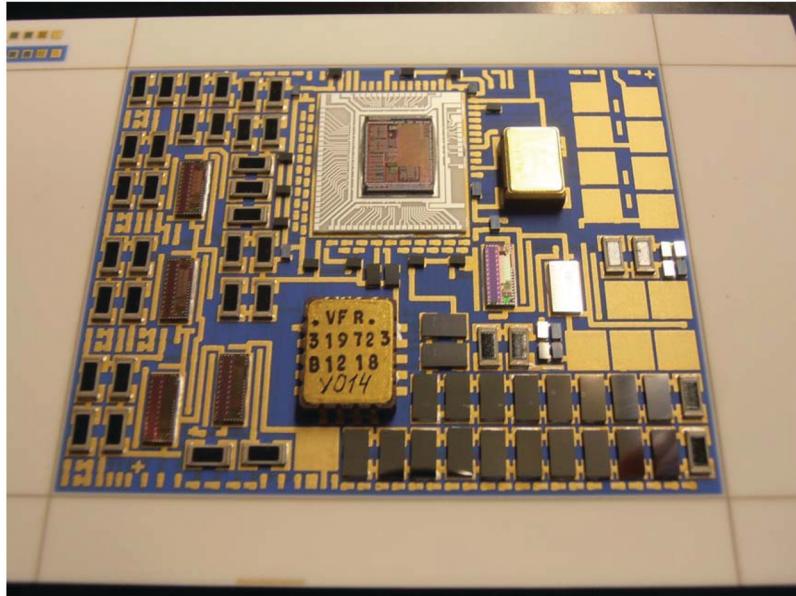
- HIGHECS ASIC
- Interposer
- Voltage Regulators
- Clock Oscillator
- Precision Resistor
- Resistors
- Capacitors

The bare die components including the silicon capacitors were attached onto the thick film pads on the alumina substrate. TVS devices were only assembled into some of the hybrid circuits.

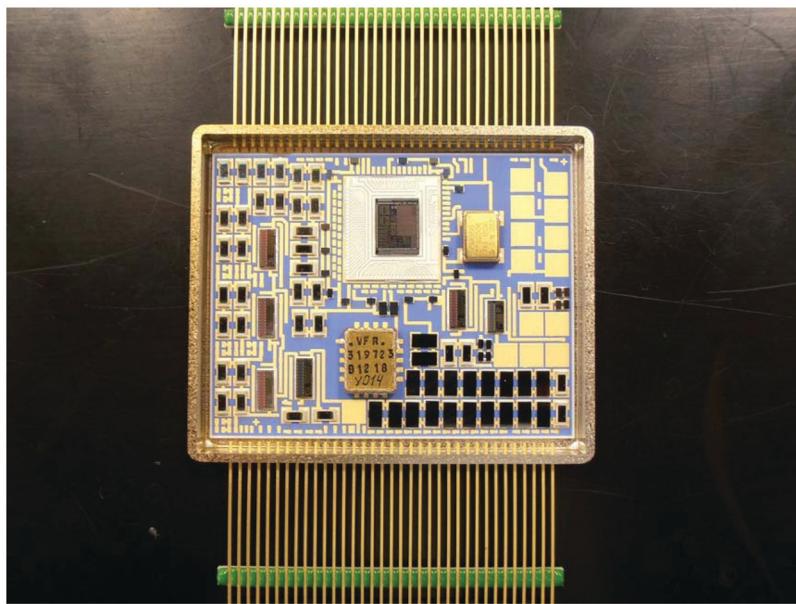
#### **3.4.1.2 Assembly of Ceramic Substrate to Metal Package**

The populated substrate was mounted into the metal package as shown in Figure 3.9. Some of these samples were populated with prototype SiC transient voltage suppressors.

A lid was resistance seam sealed onto the metal package in an inert atmosphere and gross/fine leak tested.



**Figure 3.8** HIGTECS populated hybrid circuit substrate.



**Figure 3.9** HIGTECS hybrid circuit mounted in metal package.

### 3.4.1.3 High Temperature PCB for Resistors

The size of the derated high temperature resistors for the frequency circuits precluded their use in the hybrid circuit. A separate high temperature circuit board was designed specifically for these high temperature resistors and the components were assembled using a high melting point solder, as shown in Figure 3.10.

### 3.4.1.4 HIGHTECS Module

The hybrid circuit and high temperature PCB containing the resistors were mounted into the stainless steel enclosure, as shown in Figure 3.11.

The connections between the leads on the metal package, connection pads on the printed circuit board and the connectors in the stainless steel enclosure were made with polyimide insulated copper wire, attached with high melting point solder.

The HIGHTECS module with the removable lid attached is shown in Figure 3.12.

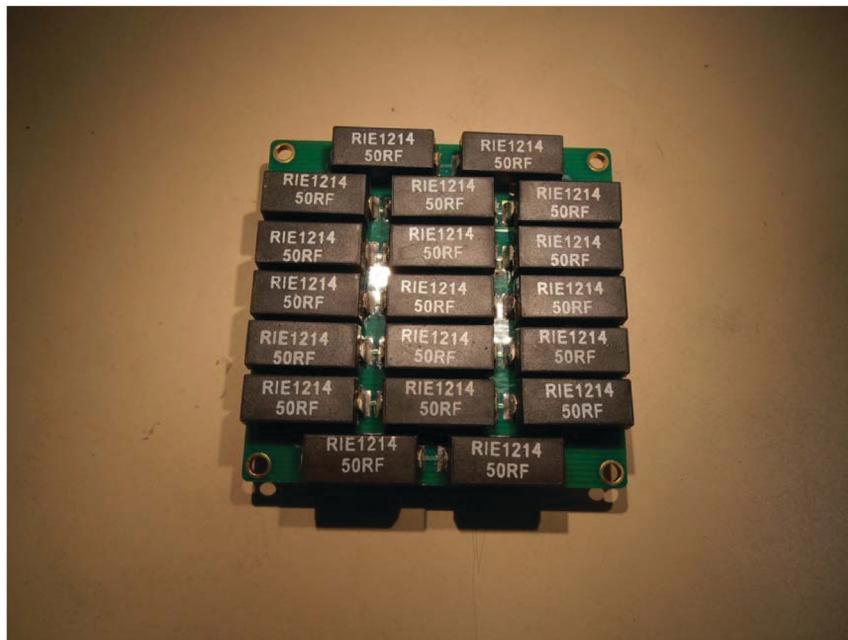
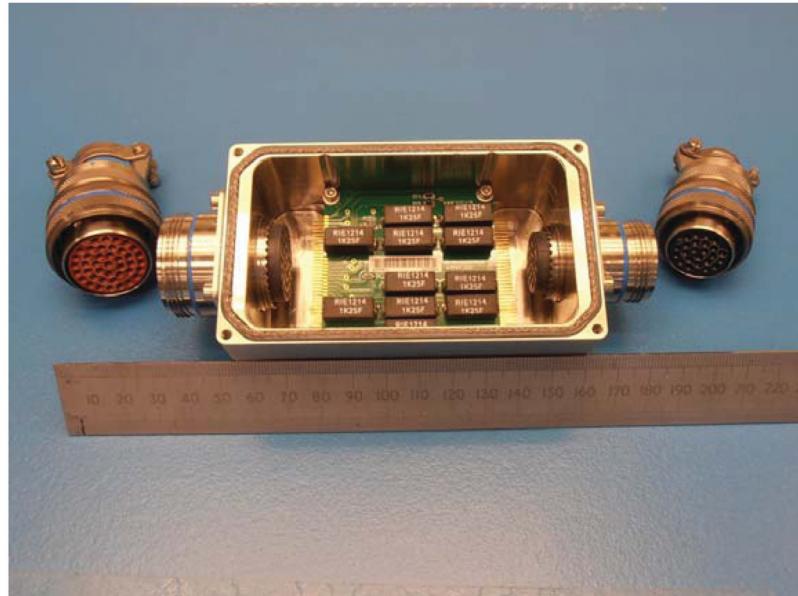
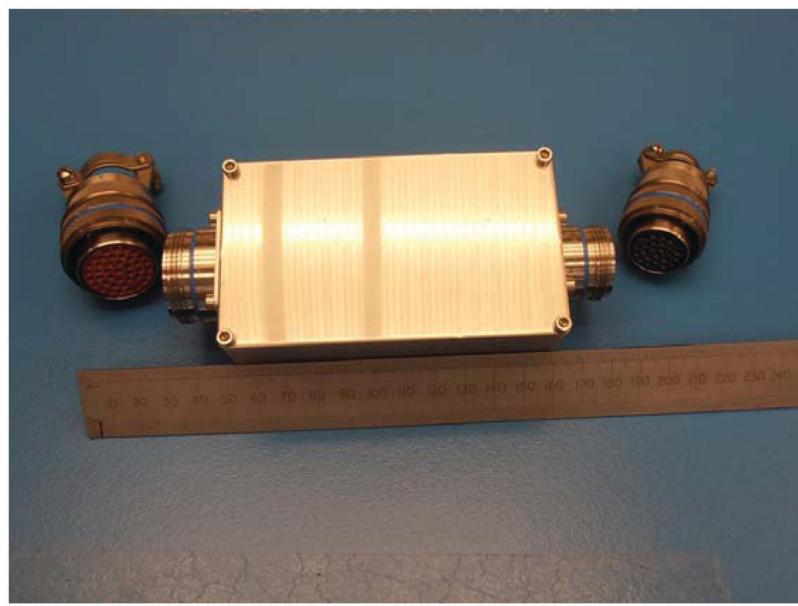


Figure 3.10 Resistors surface mounted onto high temperature printed circuit board.



**Figure 3.11** Stainless Steel enclosure with mounted PCB and hybrid circuit.



**Figure 3.12** Stainless steel enclosure with lid incorporating EMI gasket.